USN | | | | | | | | | | 10EC63

Sixth Semester B.E. Degree Examination, July/August 2022
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast THREE questions from Part-A and any TWO questions from Part-B.***

PART – A

1 a. Mention the voltage requirements of an enhancement NMOSFET to work in different regions of operation. Derive an expression for current I_{ds} in linear region of operation with necessary diagrams. **(10 Marks)**

b. Design the circuit of Fig.Q1(b) so that the FET operates at $I_{ds} = 0.4$ mA and $V_d = 0.5$ V. The NMOSFET has $V_{tn} = 0.7$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $L = 1\ \mu m$, $W = 32\ \mu m$ and $V_{DD} = 2.5$V.

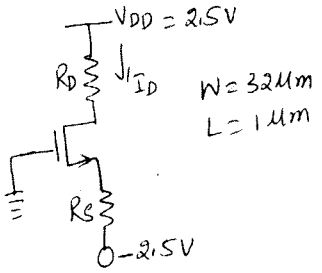

Fig.Q1(b) **(10 Marks)**

2 a. Explain the graphical derivation of CS MOSFET amplifier transfer characteristics with suitable diagrams. **(10 Marks)**

b. Explain the working of single stage common gate MOSFET amplifier circuit. Define R_{in}, V_o, A_{Vo}, A_V and G_V for the same circuit. **(10 Marks)**

3 a. Compare NMOSFET and BJJ with respect to the following parameters:
(i) Active region voltage values (ii) Current expression in the active region
(iii) Low frequency T-model (iv) Transconductance g_m **(08 Marks)**

b. Explain with suitable diagram current mirror and current steering circuits. **(08 Marks)**

c. Explain briefly cascade amplifiers. **(04 Marks)**

4 a. Design the current of Fig.Q2(a) to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel lengths of 1 μm , channel widths of 10 μm , $V_t = 0.7$ V and $k'_n = 200\ \mu A/V^2$, what is the lowest possible value of V_0? Assume $V'_A = 20V/\mu m$. Find the out resistance of the current source. Also find the change in output current resulting from a +1V change in V_0.

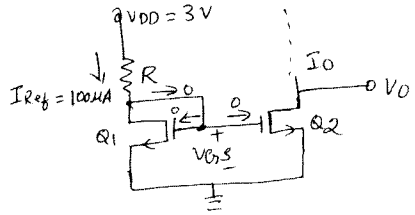

Fig.Q2(a) **(10 Marks)**

b. Explain the working of CMOS implementation of common source amplifier and define the voltage gain. **(10 Marks)**

5 a. Explain the operation of BJT differential pair configuration. **(10 Marks)**

b. Explain the frequency response of current mirror loaded MOS differential pair circuit. **(10 Marks)**

PART – B

6 a. Explain how noise reduction and band-width extension can be achieved using negative feedback with necessary diagrams and expressions. **(10 Marks)**

b. Explain the ideal structure of a series-series feedback amplifier with figures and expressions. **(10 Marks)**

7 a. Design an inverting op-amp circuit to form the weighted sum V_0 of two inputs V_1 and V_2. It is required that $V_0 = -(V_1 + 5V_2)$. Select values for R_1, R_2 and R_f so that for a maximum o/p voltage of 10V, the current in the f/b resister will not exceed 1 mA. **(06 Marks)**

b. Explain different amplifiers with neat diagrams. **(08 Marks)**

c. Explain briefly Sample and Hold circuits. **(06 Marks)**

8 a. Explain the following characteristics of a logic family. **(06 Marks)**

b. Write about the dynamic operation of CMOS inverter with necessary diagrams and expressions. **(10 Marks)**

c. Draw the CMOS schematic and AOI implementation for

$$Y = \overline{AB + CD}$$ **(04 Marks)**

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